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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yeo, *et al.*	Docket No.:	TSM03-0926
Serial No:	10/685,938	Art Unit:	2891
Date Filed:	October 15, 2003		
Title:	Dummy Pattern for Silicide Gate Electrode		

CERTIFICATION OF FACSIMILE TRANSMISSION

I hereby certify that the following papers are being transmitted by facsimile to the U.S. Patent and Trademark Office at (571) 273-8300 on the date shown above:

- Certification of Facsimile Transmission (1 page)
- Notice of Appeal (2 duplicate pages)
- Pre-Appeal Brief Request for Review (1 page)
- Pre-Appeal Brief Request for Review Comments (5 pages)

Respectfully submitted,

Kristin R. Hayes
Legal Assistant

Confirmation Respectfully Requested

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)	
TSM03-0926	

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on January 19, 2006

Signature: /Hayes/

Typed or printed name: Kristin R. Hayes

Application Number	Filed
10/685,938	October 15, 2003

First Named Inventor: Yeo, et al.

Art Unit	Examiner
2891	Farahani, Dana

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).
Note: No more than five (5) pages may be provided.

I am the

- [ ] applicant/inventor.
- [ ] assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96)
- [X] attorney or agent of record. Registration number 46,836
- [ ] attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 _____

/Roger C. Knapp/
Signature
Roger C. Knapp
Typed or printed name
972-732-1001
Telephone number
January 19, 2006
Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

[X] *Total of 2 forms are submitted.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Yeo, *et al.*	Docket No.:	TSM03-0926
Serial No.:	10/685,938	Art Unit:	2891
Filed:	October 15, 2003	Examiner:	Farahani, Dana
For:	Dummy Pattern for Silicide Gate Electrode		

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Dear Sir:

Claims 1, 2, 4, 5, 9, 11, and 12-16 have been rejected under 35 U.S.C. § 102(e) as assertedly being anticipated by U.S. Patent Application Publication No. 2003/0011032 A1 to Umebayashi (hereinafter "Umebayashi"). Claim 3 has been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 2 above, and further in view of U.S. Patent No. 6,686,248 B1 to Yu (hereinafter "Yu"). Claims 6, 7, 17, and 18 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 6,873,051 B1 to Paton et al. (hereinafter "Paton"). Claims 8 and 19 have been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 6,797,641 B2 to Holmes et al. (hereinafter "Holmes"). Claim 10 has been rejected under 35 U.S.C. § 103(a) as assertedly being unpatentable over Umebayashi as applied to claim 1 above, and further in view of U.S. Patent No. 5,994,759 to Darmawan et al. (hereinafter "Darmawan").

Independent claims 1 and 13 are the subject of this pre-appeal request. Applicants reserve the right to further argue other claims in an appeal brief.

1. Undisputed Facts

- Claims 1 and 13 are the only pending independent claims.
- Claim 1 recites the limitation "at least one dummy silicide structure formed on the semiconductor substrate."
- Claim 13 recites the limitation "at least one dummy silicide structure formed on the substrate."
- Figure 5A of Umebayashi illustrates a right-most structure 71 formed over an isolation region.
- Umebayashi refers to the right-most structure 71 as a "dummy gate pattern 71." (See Umebayashi, paragraph 66.)
- Figure 5A of Umebayashi is a two-dimensional cross-sectional view of a DRAM.
- In the context of the present application, a dummy structure "does not perform a logical function for the circuitry contained on the semiconductor chip." (Applicants' Patent Application, paragraph 32.)

2. Issue

The issue in the application is whether or not the right-most structure 71 in Figure 5A is a dummy structure in the context of Applicants' claims, *i.e.*, a structure that "does not perform a logical function for the circuitry contained on the semiconductor chip."

3. Discussion

Umebayashi itself makes it clear that the right-most structure 71 is **not** a dummy structure that "does not perform a logical function for the circuitry contained on the semiconductor chip." Regardless of the fact that Umebayashi refers to the right-most structure 71 as a dummy gate pattern 71, Umebayashi explicitly teaches that the dummy gate pattern 71 is a word line, *i.e.*, an active element for the circuitry contained on the semiconductor chip.

Generally, the process disclosed in Umebayashi involves forming dummy gate patterns 71 as described in paragraph 62 with reference to Figures 4A-4B. The dummy gate patterns 71 are used as masks to form the low concentration diffusion layers 72 (*e.g.*, the source/drain regions). (Umebayashi, paragraph 63.) An insulating film 18 is deposited over the dummy gate patterns 71 (Umebayashi, paragraph 68, Figures 5A-5B), and a CMP process is performed to expose the top of the dummy gate patterns 71 (Umebayashi, paragraph 71, Figures 6A-6B). Thereafter, the material of the dummy gate patterns 71 is replaced. (Umebayashi, paragraph 72-74, Figures 7A-7B.) Hence, the name "dummy" gate patterns refers to the fact that the gate patterns are removed and then later replaced. Finally, Figure 8 of Umebayashi illustrates the final configuration wherein it is shown that the right-most dummy gate pattern 71 of Figure 7A is electrically coupled to other circuitry, such as the transistor formed immediately to the left of the right-most dummy gate pattern 71 via the electrodes 87 and 88 and the first wiring 41.

It should be noted that with reference to Figure 5A, Umebayashi also refers to the second right-most structure 71 as a "dummy gate pattern 71" even though it is clearly an active transistor. As discussed above, the word "dummy" simply refers to the fact that the dummy gate is replaced in a later processing step.

In fact, Umebayashi explicitly states that the dummy gate pattern 71 is actually a word line. This is clearly evident from a reading of the entire reference. Umebayashi states that, in reference to Figure 1, "[t]he trench 81 formed in the first interlayer insulating film 18 is disposed on the element separating region 12 of the logic region, and a *word line* 84 is formed within the trench 81." (Umebayashi, paragraph 39.) (Emphasis added.) The word line 84 of Figure 1 corresponds to the dummy gate pattern 71 on the right-hand side of Figure 5A. Thus, *the dummy gate pattern 71 of Umebayashi is not a dummy structure as recited in Applicants' claims 1 and 13.*

These arguments were made by the Applicants in previous responses, including Applicants response under 37 CFR §1.116, dated November 29, 2005. In response to Applicants' arguments, the Office Action stated:

> Applicants argue that the dummy gate of the [Umebayashi] reference . . . is not a dummy gate . . . However, [Umebayashi] discloses in figure 5A, that the gate has separating trench isolation right beneath it. Therefore, it does not function as a conventional gate, hence it is a dummy, or non-functional gate. Even though, the gate is connected to connection 41, it does not play a role in device operation. Note that it is surrounded on all sides (except the top) by insulators 21 and 76 (of figures 5A) and 12 (of figure 3A), and it does not in any way acts as an active circuit element such as an active gate, which includes corresponding source and drain regions would.

(Office Action, pages 5-6.)

Applicants respectfully submit that this response contained in the Office Action is off point and appears to be operating under the misconception that the only type of active circuit element is a transistor. This is simply incorrect. Applicants have not and do not assert that, at the particular place the cross-section was taken, the right-most dummy gate pattern 71 illustrated in Figure 5A is a transistor having a gate and source/drain regions formed on either side of the gate.

Rather, Applicants assert that the dummy gate pattern 71 is a ***word line*** as discussed above. As such, it does not need to correspond to a "conventional gate" complete with corresponding

source and drain regions. Furthermore, as a word line it is appropriate and even desirable that it have a separating trench isolation beneath it.

The Office Action also appears to be neglecting to consider the entire design of a memory array. In a typical memory array, a word line extends across multiple memory cells, wherein adjacent memory cells are separated by isolation regions. Accordingly, a word line does not typically have source/drain regions formed on either side for the entire length of the word line. (In fact, if this were true, then the entire word line would form only one large transistor. Obviously, this is not the case.) The cross-section illustrated in Figure 5A of Umebayashi is merely a portion of the entire memory array, wherein the right-most dummy gate pattern 71 of Figure 5A extends into and out of the page. As the right-most dummy gate pattern 71 (*i.e.*, the word line 71) extends into and out of the page, it acts as a gate of a transistor for other adjacent memory cells. Simply put, the right-most dummy gate pattern is not a "dummy silicide structure" as recited in Applicants' claims 1 and 13.

Respectfully submitted,

January 19, 2006
Date

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